Minutes of LHC-CP Link Meeting 15

Subject	:	LHC Controls Project

Date	:	17th July, 2001

Place	:	936-Conference Room

Participating Groups	:	EST-ISS	no representative,
		LHC-ACR	apologies,
		LHC-ECR	no representative,
		LHC-IAS	J. Brahy,
		LHC-ICP	apologies,
		LHC-MMS	no representative,
		LHC-MTA	apologies,
		LHC-VAC	I. Laugier representing R. Gavaggio
		PS-CO	F. Di Maio,
		SL-AP	no representative,
		SL-BI	no representative,
		SL-BT	apologies,
		SL-CO	apologies,
		SL-HRF	no representative,
		SL-MR	R. Billen,
		SL-MS	no representative,
		SL-OP	M. Lamont,
		SL-PO	Q. King,
		ST-MO	P. Sollander.

Others	:	F. Calderini (Alarm Sub-Project),
		A. Daneels (Project Planning),
		R. Lauckner (Chair),
		R. Schmidt (MPWG)

Distribution	:	Via LHC-CP website: **http://cern.ch/lhc-cp**
		Notification via: **lhc-cp-info@cern.ch**

Agenda	:	1. Matters arising from previous meeting
		2. LHC-CP News R. Lauckner
		3. Role of the TCR P. Sollander
		4. Front Ends Architecture P. Ribeiro
		5. AOB

1. **Matters arising from previous meeting**

No follow up had taken place concerning milestones for the QRL alarm and database activities during 2002. This is moved to the long term actions.

R. Lauckner and M. Lamont had had discussions with R. Saban and R. Schmidt concerning the installation database. This subject had been included in a presentation to the previous TCC concerning hardware commissioning for which R. Saban will be responsible. R. Saban will present the subject at a future LHC-CP meeting.

The ORAPCR committee has not yet started work so the actions concerning the definition of operational data and the launch of work for the QRL databases are moved to the long term actions.

2. **LHC-CP News   R. Lauckner**

The LTI and CNGS Controls Review had taken place on July 10th and the slides will be posted on the web: http://cern.ch/lhc-cp/lti_cngs/Agenda.html. The major outcomes had been the lack of progress in preparing cabling, racks and communication infrastructure and a high level of concern for the resources and software infrastructure for the Control Room Software. There was also clear disagreement concerning the API for distributed applications. The organisers are preparing a report and recommendations.

M. Lamont reported briefly on a visit to the Laboratoire d'Automation de Grenoble to discuss a possible collaboration on feedback control systems. The LAG place students for 4 months and doctoral studies as well as providing consultancy.

R. Lauckner presented a proposal for the LHC-CP work and meetings until the end of 2001. Formal planning of the activities is still not in place but nevertheless decisions and actions are clearly urgent in several areas.

LHC-CP Calendar		
Alarm System Preliminary Requirements	11-Sep-01	M. Tyrrell
Installation Databases Report	11-Sep-01	R. Saban
Components Recommendations	25-Sep-01	P. Gayet
Post Mortem Requirements	25-Sep-01	J. Wenninger
Back-Ends for LHC	9-Oct-01	P. Charrue
Slow Timing Functional Specification	9-Oct-01	G. Beetham
Future Front Ends Recommendations	23-Oct-01	P. Ribeiro
Project Middleware Standards	23-Oct-01	R. Lauckner
Operational data requirements	6-Nov-01	R. Billen
Non PO function generator requirements	20-Nov-01	E. Ciapala
Functional Specification for Analogue Signals	20-Nov-01	E. Ciapala
Slow Timing H/W and S/W Interfaces	4-Dec-01	G. Beetham
Sector Test Preliminary Planning	4-Dec-01	A. Daneels
Post Mortem Functional Specification	18-Dec-01	J. Wenninger
Real Time Control	18-Dec-01	M. Lamont

G. Beetham and M. Vanden Eynden have started work on the Function Specification for the slow timing. The documentation of other deliverables associated with this programme will be clarified with M. Vanden Eynden.

ACTION: M. VANDEN EYNDEN

3. Role of the TCR   P. Sollander

P. Sollander introduced this topic explaining that the future role of the TCR during the operation of first the cryogenics and QRL and later the LHC machine would not be different from today's activities. The TCR operator's basic activity is monitoring of events concerning the CERN technical services and peripheral systems such as Safety, Control System, Control Network and Cryogenics. The events are:

_ An alarm from the CERN Alarm System (CAS)

_ A telephone call

The following actions may be taken in response to these events:

_ Reset faults and / or restart system via the Control System

_ Call a piquet

_ Perform the first line intervention on selected systems

_ Co-ordination of Troubleshooting for Major Perturbations

The responsibilities of the TCR are targeted on minimising downtime for the accelerators and experiments, avoiding damage to equipment and injuries to people.

A project, "Gestion Technique des Pannes Majeurs" (GTPM), had been launched in 2000 to improve the recovery procedures following a major breakdown. The first system being studied is the SPS accelerator. Operators and specialists from those machines are elaborating the recovery procedures to be followed from the TCR and PCR. The aim is to reduce downtime by implementing optimised and co-ordinated actions from the 2 control rooms.

Future LHC systems will be integrated into the monitoring framework of the TCR using the existing "TCR Control Desk" (TCD) procedure. This is systematically applied to all extensions from a few extra I/O points for an existing application to the introduction of major systems such as the SPS cooling and ventilation system. Such changes must be planned, with a few months foreseen for the introduction of major systems. The procedure starts with a request to the TCR and the preparation of an Excel Form, the TCD Request, to prepare the actions to be carried out to add the new system. The ST/MO group then executes all the work to integrate the system into their infrastructure. The request is closed after an acceptance test.

Finally P. Sollander described the Controls Architecture of the TCR. Today this is based on various components: Smart sockets middleware, UMMI synoptic tool, the CAS and JavaGuils. These are being migrated into the environment provided by the PVSS product.

R. Lauckner and Q King asked about specific systems being monitored. The first LHC system to be integrated is the cooling and ventilation at SM18. The CV system and the vacuum for String 2 are monitored via a few alarms. Concerning the LEP cryogenic systems a few alarms were monitored. Previously a cryogenic application had been deployed in the TCR but later this was moved to the cryogenic control room.

Ronny Billen asked about activities carried out under the C168 contract. Peter Sollander explained that this covers both maintenance and development work. UMMI maintenance and CAS database updates are now the responsibility of the contractor. For the database work he collects update requests, enters them into the system and performs the monthly update of the on-line database. So far he has not been directly involved with the TDrefDB.

F. Calderini queried the use of PVSS as the Alarm MMI. P. Sollander explained that this was a very strong user requirement. PVSS was a strategic choice for the TCR and it will open new functionality for the Alarm users.

In other discussions it was reported that the future of the JavaGuils application has yet to be decided in the light of the introduction of PVSS. The choice of PVSS as the SCADA system for the LHC machine and technical services will open up possibilities for native integration of future systems.

4. Front End Architecture   P. Ribeiro

P. Ribeiro, leader of the SL-CO Front End section, reported that he has been working with P. Gayet to complete the survey of Front End systems. He recalled the previous report from P. Gayet that covered the architecture of slow control systems around the LHC. His purpose was to extend the view into those systems anticipating the use of "classic" Front Ends.

He continued by reporting his experience working on the LHC-ICP system for Quench Protection at String 2. He had undertaken this work in order to learn more about integration of systems. The requirement was to connect a FIP node equipment controller the AMC, an industrial supervisor as an OPC client on Windows NT and Oracle running on Solaris.

A diskless power PC Lynx OS VME front end and a Linux Boot Server were chosen to perform the integration, familiar systems at SL. An OPC server was built running on the PCVue database host. This was implemented as a threaded process, AmcOPCServer, another thread running a custom smart TCP/IP socket communication towards the Front End. On the Front End a complementary threaded process, mpgate, was developed, Threads implement the FIP driver and a remote user terminal, system monitoring, the smart TCP/IP connection. Other threads implement the application, these were developed by J. L. Gomez Costa. 30 000 lines of code have been developed by P. Ribeiro to implement the framework while the application represents 40 000 lines of code. The work under WNT had been relatively simple using existing C++ class libraries.

Several factors dictated the choice of a custom Front End solution as opposed to a PLC. The existing architecture of the AMC - a single board radiation resistant FIP node without an operating system, a requirement to connect directly to the Oracle server in order to improve reliavbility, and the required support for GPS and IRIG B.

He completed his presentation with a review of the current requirements for classic Front Ends at the LHC. The PO group is advancing with work just starting at the Front End level to integrate the Digital Function Generators. These are connected on a 2.5 Mbit WorldFIP link. It is not clear how the real-time traffic can be carried to the centre and the timing interfaces are not yet defined. BI group will use VME/Lynx OS Front Ends. The work is well advanced and the system will be deployed for trajectory monitors in the TI8 transfer line, commissioning in 2004. Again the question of real-time traffic support above the Front End is not yet addressed. Electronics has been developed at Triumph in Canada. BT group have a wide variety of Front End needs. Industrial systems for slow controls, a custom system for accelerator timing, VME today, and commercial waveform acquisition systems to replace the current VXI solution at SPS. In order to regulate their equipment in the LHC communication is required between these 3 systems. No solution is available yet to meet this requirement. Extension of support to cover compact PCI (cPCI) solutions for timing hardware could be considered. Finally the RF group have started to study their slow controls needs.

At the moment the FE section are studying the users requirements and proposals with a view to understanding how much diversity they can support. He pointed out the retention of Lynx OS was a key element in providing stability for users who also have responsibility for existing SPS systems. This OS was migrating towards LinuxWorks and appears to be a healthy niche system. VME is a stable platform with stable sales and is well mastered by CERN developers. Intel based VME is being selected as a standard by the EP loan pool. cPCI could be a future supported option but this depends on the additional complexity and the resources in the FE section.

R. Lauckner reminded the meeting that the project mandate included the reduction of diversity and duplication of effort in the LHC Control System. There was clearly a lot of work to do before the end of October concerning the architecture of these systems.

Q. King remarked on the importance of the Middleware issue as demonstrated by the AMC project. This confirms his current priority for clarification of this area. He also pointed out that the cPCI bus speeds are higher than VME and asked how this would evolve. P. Ribeiro replied that the VME bus speed was a bottleneck but that higher speeds were planned. R. Lauckner said that this issue was not of direct concern. Highest bus speeds were needed by the BI applications and the group was in favour of using VME for their LHC systems.

R. Lauckner requested clarification on the policy of the EP loan pool. They are interested in classic VME and also the faster, larger format, bus. The LHC detectors will use classic VME and this will be followed up by the FE team.

P. Ribeiro also explained the issues surrounding the use of a PLC or a custom Front End for the integration of the device controller, AMC. The complexity of the task required the full flexibility of a custom Front End. The complete system would have to be re-engineered if PLCs are to be used.

5. AOB

There was no further business.

Long Term Actions	People
Milestones for Alarm and Database work for QRL	A. Daneels
Establish Real-time sub-project.	R Lauckner
Establish Post Mortem sub-project	R. Lauckner
Attach leaves to EDMS tree	All, M. Vanden Eynden
Clarify Middleware services to be used by LHC-CP	Core Team

Reported by R. Lauckner

Role of the TCR

TCR Systems under Control

Electricity	Safety
HT, MT, BT, Energy Consumption, etc.	Fire, Gas, Emergency Stop, ...

Water
Pumping Stations, Raw, Prim, Chilled, Demi, ...

Control Hardware
Front ends, Servers

Thermal
Air-conditioning, Ventilation, Heating

Control Network

Vacuum
Pumps, Pressures

Cryogenics
Pumps, Temperatures

TCR
- 24h/day
- 365days/year
- Monitoring
- On-site interventions and stand-by services
- Troubleshooting coordination

TCR Responsibility

- Accelerators & Experiments support
- Involved in Safety monitoring
- CERN infrastructure and equipment protection

	Process	Equipment	People
Magnitude	Accelerators Experiments	X * Billions CHF	10 000
Target	No downtime (hours)	No damage	0 injuries or fatalities

TCR Monitoring Requirements

- What do you want ?
- Functional Analysis
  - Which systems should work ?
  - What should they deliver ?
  - What are the interfaces & dependencies between the systems ?
- Dysfunctional Analysis
  - What to do when all goes wrong ?
  - Can the system become dangerous in case of functional or transmission path errors ?
  - Will the TCR know if some functions are not available ?

TCR integration concept

GTPM

- Monitoring mandate and specification
  - TCR role, responsibilities, procedures,
  - operators and equipment specialists
- Detailed specification of monitored points **TCD**
  - Alarms, logging, mimics, commands
  - operators, equipment specialists and IN staff
- Implementation in control system

  PVSS II
  - Configuration, view development, testing
  - ST/MO/IN + operators + C168
    - Limited resources -> only planned integration tasks!

Method **GTPM**

- Gestion Technique des Pannes Majeures
  - Reduce SPS restart time after major breakdown
    - Definition of roles, responsibilities, procedures
    - Improve collaboration PCR-TCR
    - Set of tools (instructions, process description, function and logic of the restart, etc.)
    - Improved operator training
    - Better system understanding
    - A structured approach, to be generalized in future projects

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TCR Control Desk **TCD**

Request to TCR

Operator contacts requestor

Data definition Results in

ST/MO internal procedure starts ...

TCR operation
- instructions
- help text definition

Cabling, PLC
- installation
- specify PLC parameters

TDrefDB
- load data in Oracle
- verify data consistency

TDS, SCADA
- generate configuration files
- restart and test processes

UMMI
- define user interface
- program and test

Data Logging
- define data
- configuration and test

CAS update
- prepare interface data
- restart process and test

Internal test
- monitoring system
- alarms

Acceptance Test and closure of request

DAVID HAY (T8063)
ROBIN MARTINI (73130 or 72301)
NEW

	Planned	Status
73130	12-MAY-2001	IN WORK

- For projects:
 - Co-ordination and follow-up by the ST/MO project linkman

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Monitoring System

- Robust and flexible
  - Based on "Functional Safety" criteria:
    - Reliability, Availability, Maintainability, Safety
- Industrial tools: SCADA, PLC, Support
- Homogeneous operational environment
  - Unique alarm & logging system
  - Mimic diagrams local or integrated **PVSS II**
  - One platform type
- Layered-based Architecture providing:
  - Modularity, Reusability of solutions
  - Shorter system integration time

Monitoring system architecture
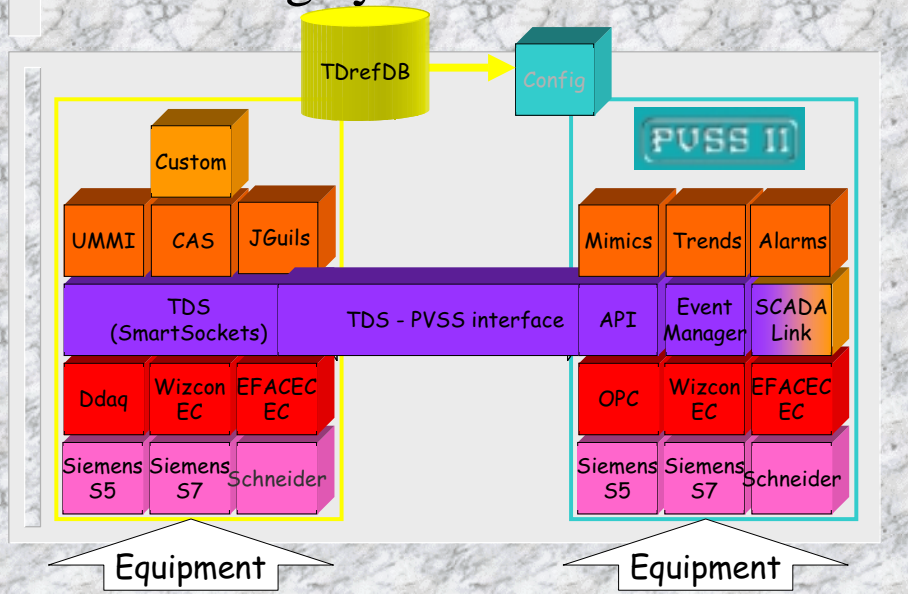
In a nutshell

- TCR already has a defined role in operation
  - We supervise the technical infrastructure today
- Role and responsibilities can be extended
  - New requests must use standard procedure
    - GTPM   definition of operational role
    - TCD   detailed data definition
    - PVSS   tool implementation
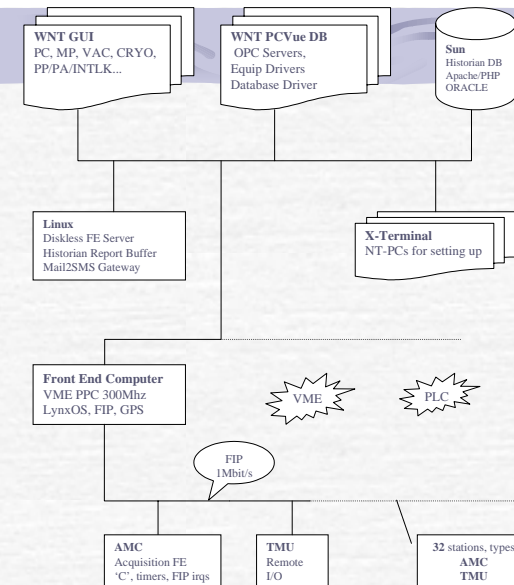- Planned request $\Rightarrow$ successful integration

Future Front-End Computers

- Introduction
- PLC applications
- Open FE needs
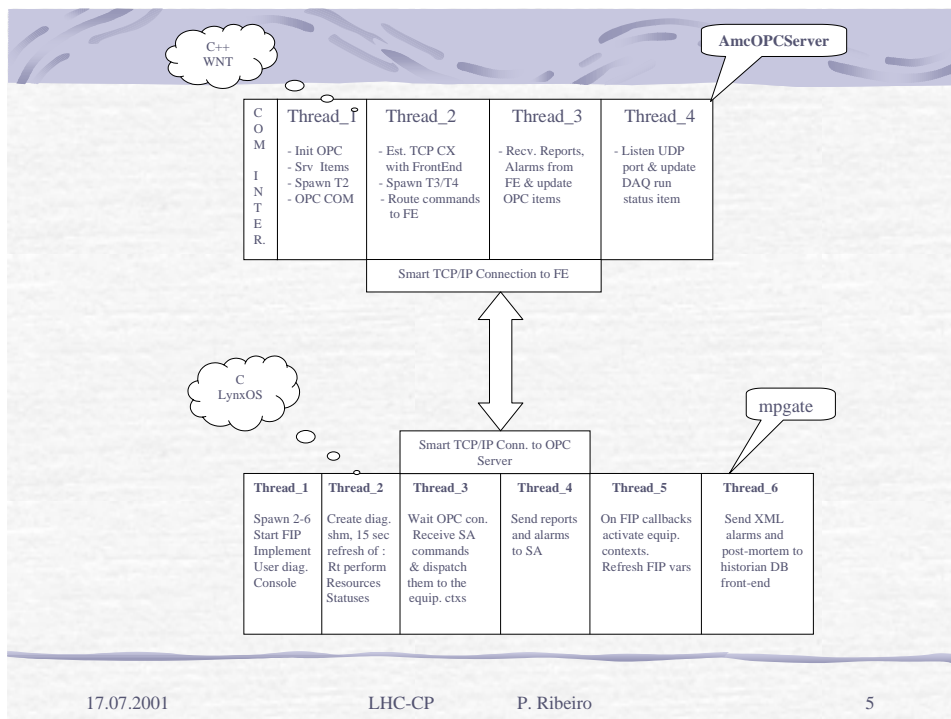- Stability vs Trends
- Strategy
- Conclusion

PLC applications

- http://lhc-cp.web.cern.ch/lhc-cp/Sub-Projects/Components/Minutes1.PDF

LHC/ICP, Magnet Protection Diagnostic System for STRING-2

- *Why VME/LynxOS for this project and not PLC ?*

  – Existing user code in C (for AMC)
  – GPS/IRIG-B
  – Direct reporting to DB
  – Looking for manpower

WNT GUI
PC, MP, VAC, CRYO,
PP/PA/INTLK...

WNT PCVue DB
OPC Servers,
Equip Drivers
Database Driver

Sun
Historian DB
Apache/PHP
ORACLE

Linux
Diskless FE Server
Historian Report Buffer
Mail2SMS Gateway

X-Terminal
NT-PCs for setting up

Front End Computer
VME PPC 300Mhz
LynxOS, FIP, GPS

VME   PLC

FIP
1Mbit/s

AMC
Acquisition FE
'C', timers, FIP irqs

TMU
Remote
I/O

32 stations, types
AMC
TMU

Slide 5

C++
WNT

C O M I N T E R.	Thread_1	Thread_2	Thread_3	Thread_4
	- Init OPC - Srv Items - Spawn T2 - OPC COM	- Est. TCP CX with FrontEnd - Spawn T3/T4 - Route commands to FE	- Recv. Reports, Alarms from FE & update OPC items	- Listen UDP port & update DAQ run status item

Smart TCP/IP Connection to FE

C
LynxOS

mpgate

Smart TCP/IP Conn. to OPC Server

Thread_1	Thread_2	Thread_3	Thread_4	Thread_5	Thread_6
Spawn 2-6 Start FIP Implement User diag. Console	Create diag. shm, 15 sec refresh of : Rt perform Resources Statuses	Wait OPC con. Receive SA commands & dispatch them to the equip. ctxs	Send reports and alarms to SA	On FIP callbacks activate equip. contexts. Refresh FIP vars	Send XML alarms and post-mortem to historian DB front-end

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Slide 6

LHC/ICP

- **OO (no)**
  - WNT code includes a set of 5 classes (OPC server framework)
  - MFC and TCP/IP wrapper classes from MS
  - 4 home made classes
  - but no systematic OO A/D

- **Code size**
  - Quite compact on WNT side due to the reuse of existing code
  - On LynxOS side 70000 lines of code 30K (me), 40K (JLGC)

- **Number of OPC Items/Data Points (45 devices)**
  - ~4700

Slide 7

LHC/ICP

- RT performance

  o OPC variables are refreshed on a 3 secs basis, 15% load on a 700Mhz PIII

  o 100ms FIP cycle, all user callbacks MUST finish before next cycle starts, includes FIP variables handling, SA reporting, DB reporting.

Slide 8

Needs PO

- SPS/Transfer Lines
  - ROCS
    - VME, CES PPC, TG8, LynxOS
- LHC (80-100 systems + PCR)
  - RTOS, RT network interface (?)
  - WorldFIP 2.5Mbps
  - GPS, TG8 (?)
  - BUS independent, but end 2001

Needs BI

- **SPS**
  - VME, CES PPC, TG8, LynxOS
- **LHC (80 systems + PCR (?))**
  - RTOS, RT network interface (?)
  - WorldFIP 31.25Kbps
  - TG8, GPS
  - DMA 30MB/s (curr ~16MB/s)
  - BUS, CO and users in favour of VME arguments being
    - BI's high slot count use (chassis price)
    - Long experience
    - Specific modules development (DAB, Triumph)

Needs BT

- Different types of front-end will be used.
- Selection criteria depend of the signals to be acquired and/or on the functionality to be realised.
- None of the solutions actually available offer the possibility to use a single approach.
- Front-end means not only hardware, but also software (OS, drivers…). Optimum and easy integration of different hardware acquisition cards has to be taken into account.

Regulation

- Pulse to pulse regulation loops have to be implemented in order to control the kick amplitude and synchronisation stability.

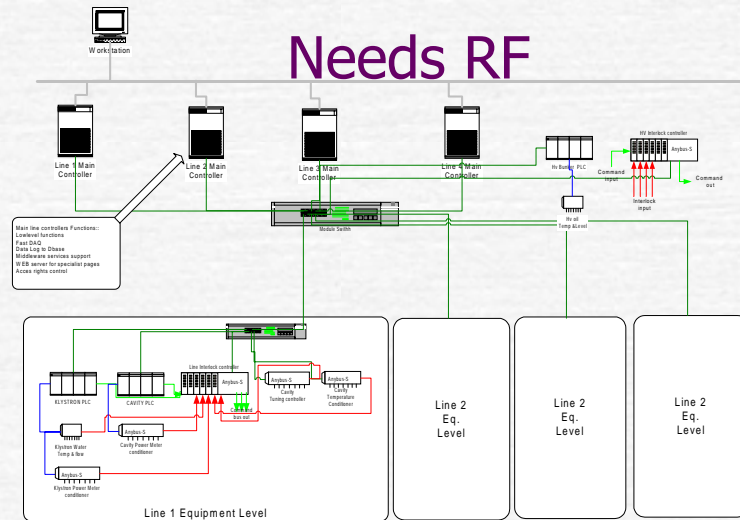| Acquisition	Analysis	Action
VXI Waveform acquisition	**VXI**	**VME** Timing **SCADA** Power supply Heater

Different type of front-end have to be involved in the regulation loops. Intercommunication?

Needs BT

- CO Fes because of slow timing (few)
- No RTOS requirement
- What if CO FE could cover Analog Acquisition and even Waveform acquisition ? (cPCI)

Needs RF

Needs EA

- VME for ever, IP Modules
- No RTOS requirement
- JAVA even at the FE level (easier with Intel)

Stability vs Trends

- Large installed base PPC's and PC's, all LynxOS
- Users want stability, best keep OS
- LynxOS (LinuxWorks) is healthy and converging towards Linux binary compatibility (VME, cPCI)
- VME keeps is market share
- EP Pool wants to standardize on VME Intel with Linux
  - Contract with supplier (Concurrent ?)
- cPCI is growing and offers new possibilities for building fast analog/waveform acquisition systems
- Would Embedded NT support be of interest ?

Strategy

- We try to answer
  - Could our VME users run on EP Pool Intel processor ?
  - Can we provide LynxOS support for it ?
  - Could we have a second FE option with cPCI ? 3U/6U/both ?
  - Can we provide LynxOS/Embedded NT support for it ?
  - Could we provide support, cPCI, for fast analog/waveform acquisition systems

Strategy'

- WorldFIP
  - Support for 31.25Kbps, 1Mbps, 2.5Mbps
  - Follow the Alsthom upgrade path (FULLFIP3)
- GPS (??)

- TG?? -> we will support
- Support for all the classical interfaces as requested

Conclusion

- A lot of work and discussions over the past 2 years

- Important to have a date for recommendation

- Is the EP Pool approach, for the VME processor a good one or should we keep independent ?