

Minutes of LHC-CP Link Meeting 26

- Subject** : LHC Controls Project
- Date** : 2nd July, 2002
- Place** : 936-R-030
- Participating Groups** :
- | | |
|---------|--|
| LHC-ACR | no representative, |
| LHC-ECR | no representative, |
| LHC-IAS | J. Brahy, C-H Sicard, |
| LHC-ICP | A. Hilaire, F. Rodriguez-Mateo,
K-H Mess, |
| LHC-MMS | no representative, |
| LHC-MTA | no representative, |
| LHC-VAC | R. Gavaggio, |
| PS-CO | F. DiMaio, |
| SL-AP | no representative, |
| SL-BI | no representative, |
| SL-BT | E. Carlier, |
| SL-CO | P. Charrue, N. Polivka, |
| SL-HRF | E. Ciapala, |
| SL-MR | R. Billen, |
| SL-MS | no representative, |
| SL-OP | M. Lamont, |
| SL-PO | Q. King, |
| ST-MA | P. Sollander. |
- Others** :
- A. Daneels (SL-DI)
 - R. Lauckner (Chair),
 - H. Milcent (QPS Controls),
 - B. Puccio, R. Schmidt (Machine Interlocks),
 - P. Gayet (Core Team),
 - M. Vanden Eynden (Core Team).
- Distribution** : Via LHC-CP website: <http://cern.ch/lhc-cp>
Notification via: lhc-cp-info@cern.ch
- Agenda** :
1. Matters arising from Previous Meeting
 2. LHC-CP News
 3. FGC Gateways Q. King
 4. QPS Controls Requirements H. Milcent
 5. Controls for Machine Interlocks B. Puccio
 5. AOB

1. Matters arising from Previous Meeting

R. Billen reported that the discussion of the global architecture of the Cooling and Ventilation control system is planned. The goal is to explore connectivity with the LHC machine control system.

ACTION: R. BILLEN, P. SOLLANDER

R. Lauckner reported that J. Lewis would present his work on the LHC Timing to the SLTC scheduled for 3rd July.

2. LHC-CP News

Nobody had any reports under this topic!

The schedule and main topics for the next LHC-CP meetings are:

16/7	QRL Baseline, Experience from RF test stands	A. Daneels, L. Arnaudon

3. FGC Gateways Q. King

The FGC gateways will connect function generators for the power converters and the RF system to the LHC Control System. Q. King explained that there will be around 80 gateways connecting around 1700 Function Generator Cards (FGC), only 1 of the gateways will be used for the RF.

He identified 4 major roles for the gateways. The 1st is to act as the communications channel between the machine IP LAN and the FGC WorldFIP segments. LHC operations will address this channel using the Controls Middleware (CMW), while specific power converter applications will implement TCP clients to export high performance expert interfaces across the LAN. The gateway will implement the Device/Property model for exploiting the FGC nodes on the WorldFIP. Traffic on the LAN will be asynchronous and serial while there will be parallel traffic on the WorldFIP.

The 2nd role for the gateway will be to receive and distribute UTC, machine timing events and telegrams from the GMT timing distribution. A CTX1 card will receive the GMT at each gateway. This card will also generate 100 Hz pulses for the WorldFIP interface. The connection will be via a short (<10 cm) cable.

The 3rd role of the gateway will be to support Real-Time control. Information derived from sensors, typically beam based information will be passed to a central FGC RT Server. This server will route the activator data to the FGCs and implement exclusive access control to each activator. The capacity of the system will allow a single floating value to be directed to each FGC every 10 ms period of the WorldFIP cycle. In the opposite direction the gateways will publish real-time information towards the FGC RT Server. LHC monitoring applications will receive this through the CMW at typical rates of less than 2 Hz. Information will include status and alarms. The gateway will also implement the circular post mortem buffers which will be protected by the gateway UPS in case of power failure.

The 4th role of the gateway will be to enable configuration management. Information to be managed would cover persistent application data such as calibration, circuit characteristics and current loop parameters. Additionally software version management will also be implemented. New FGC software versions will be loaded through the gateway, essential for releasing new versions to 1700 installations.

Q. King explained that identity management will be performed on all FGCs and associated material using Dallas identity chips. About 40000 items will be tagged within the LHC powering system and the associated Oracle inventory will be kept up to date by the gateways, possibly via a central Unix application since Oracle access may not be possible from LynxOS. Configuration and identity management will help to reduce the complexity and time necessary for repair and maintenance work in the same location as the hardware, which will be installed in underground radiation areas.

The FGC Device/Property model will contain at least the 3 classes: gateway, FGC RF and FGC PO. A class will define all the properties for the devices belonging to the class, as well as the published data set. Properties will have associated typed data and methods for set and get. Operational properties will be accessible through the CMW, while expert properties will not be visible. Q. King explained that the properties for all the classes will belong to a common property tree but each class would only implement a sub-set of the tree.

Finally Q. King gave a demonstration of the prototype FGC web site that describes the prototype FGC used in SM18. This will be extended to be multiple class; FGC definitions will be held in XML. From these a Pearl program will generate database entries, documentation, and software header files and classes. These could include a Java class API for access via the CMW. Open questions remain concerning the nature of the client interface to be implemented and type conversion from FGC command response strings to binary types in the LHC operation clients.

In reply to a question from P. Charrue concerning configuration Q. King said that about 30 FGC nodes would be attached to a FIP segment. It may not be necessary to have an on-line Oracle configuration service to support the operation of these systems. He would consider copying the information out to files and performing operational support via these files.

R. Schmidt asked if the Dallas ID chips would be accessible when the system is in operation. Q. King confirmed that these will be visible on-line through the gateways.

Concerning other applications for the FGCs Q. King stated that work is only being targeted on the LHC. Components will become obsolete in 1 – 2 years so after the bulk orders which will only include known requirements and spares it will become necessary to re-design the FGCs for future applications.

R. Schmidt warned that equipment such as the FGCs to be installed in the RRs must be qualified for that radiation environment and work is still in progress to estimate the doses to be expected. Q. King said that 2 radiation test campaigns had been carried out in TCC2 with somewhat inconclusive results and another test is planned for next year. All SRAMS will be protected by EDACs as single event upsets are expected in the RRs.

Frank DiMaio pointed out that binary data transfer would give better performance in the CMW and performance could also be improved by grouping transactions in the middleware. This has already been done at PS. Q. King said that currently the gateway is a bottleneck, critical factors are the WorldFIP interface software and the aging CPUs.

4. QPS Controls Requirements H. Milcent

H. Milcent started his [presentation](#) by insisting that the key role of the Quench Protection System, to prevent damage to the superconducting components (coils, busbars and leads) of the magnet system, would not depend on software or any other component of the associated control system. The control system will provide monitoring of the QPS system and the magnets and for experts the commands for testing the system when it is not performing its primary role. Nevertheless the correct functioning of the control and monitoring will be critical for LHC commissioning and operation.

There are 3 main areas of responsibility associated with QPS control. The ICP group will take responsibility for the device side of the QPS gateway, the fieldbus and the controllers connected to the fieldbus. The latter are the Quench Protection System Acquisition and Monitoring Controller (DQAMC) and the Quench Protection Acquisition and Monitoring Controller for Energy Extraction Systems (DQAMS). The IAS group will be responsible for the other side of the gateway and the supervision layer. Integration tools: logging, alarm, post mortem are being followed up by the LHC-CP. Other teams associated with the QPS are the machine protection project and the LHC operations group.

Around 2077 controller crates with a total of about 70000 I/O channels will be distributed around the tunnel and underground areas. Crates will acquire data at 100Hz and timestamp it with 1 ms precision. If an event occurs they will internally buffer the associated data; they will have 10-minute UPS autonomy. Up to 50 nodes will be installed on a WorldFIP segment that will operate with a 100 ms microcycle. They will be part of the power permit chain.

There will be 35 QPS gateways, located in UAs and RRs, carrying up to 2 WorldFIP segments each with up to 50 crates. After an event each crate will provide up to 10 kB of data which must be buffered in the gateway if it cannot be sent onwards for analysis and storage. The gateway must also provide the time stamping reference to the crates via the WorldFIP. The gateway must implement access to the crates for test mode commands and will be the interface towards the Alarm, Logging and Post Mortem facilities. Supervision for experts and operators and summary power permit information for the Machine Interlock system will also depend on the gateway.

The QPS supervision will be required for system experts for commissioning and during operation. The QPS expert will also need access to LHC alarm, post-mortem and logging information. In turn the QPS system will generate data for LHC operators at the level of the gateway and define techniques to diagnose events.

Hardware testing for equipment to be installed in sector 7-8 will start on the surface in the first half of 2004. Installation will start in May 2004 and will last 2 years. Commissioning of sector 7-8 will require the QPS and controls to be fully functional; this activity starts in March 2005.

H. Milcent gave detailed information about resources and dates for the realisation of the QPS controls. In summary the control system must be progressively available during 2004. Full operation will be needed from 2005 onwards.

R. Lauckner asked about the required reliability of the control system. F. Mateos - Rodriguez said that control system faults would not cause a beam dump. It is very important that the system will be able to buffer and store the diagnostic information from the crates relating to an incident even in the event of a power failure. Responding to P. Charrue he said that quenches would typically involve a few controllers, a maximum of around 10, whose data must be reliably archived.

H. Milcent responded to questions about the choice of the gateway platforms. This choice will be based on requirements. The decision is converging on an SL VME front end although the LHC-IAS EtherFIP bridge is still being considered. M. Vanden Eynden remarked that the VME procurement could be an option to the existing volume of about 300 systems. Q. King pointed out that if this choice is made then additional CTX1 cards would be required to provide the UTC time references.

P. Gayet asked about data rates outside of incidence periods. H. Milcent said that there will be regular reading of a small amount of information, volumes will be controlled by filtering techniques.

5. Controls for Machine Interlocks B. Puccio

B. Puccio [presented](#) the current view of Controls Issues for the Machine Interlocks System. He explained that this also covers some SPS needs. The Machine Interlocks are a component of the machine protection system that also includes QPS, Beam Loss Monitors, Collimators and the Beam Dump. There are 2 interlocks the Powering Interlock and the Beam Interlock. There are links between the protection sub-systems and power converters, controls, injection, RF, experiments, vacuum, access, warm magnets, and cryogenics systems. Most of these are hardware links.

The powering interlock generates the permission condition for magnet powering and if necessary aborts the power converters and (if an extraction system is included in the circuit) requests an energy dump after a quench. The system must be robust with response times in the range of several ms – PLCs are well suited for this task. The LHC is divided into powering sub-sectors. Usually a sub-sector is associated with a continuous cryostat and has an associated Power Interlock Controller (PIC). Arc cryostats have a PIC at each end.

The Beam Interlocks must be fast and safe. Response times are at the μ sec level and logic must be hardwired. The beam interlock system will be the external trigger for the beam dump. If a critical condition arises the system will dump the beam in 2 turns (178 μ s). The hardware will be embedded in a host with a technology still to be chosen, candidates are VME, PLC and cPCI.

The major roles of the Control System will be:

- Monitoring the Interlocks
- Providing time stamping synchronisation
- For the Beam Interlock: supplying machine status (energy and intensity)
- For the Powering Interlock: communicating components of the Power Permit Condition

The energy information is required by the beam loss monitors and is safety critical.

B.Puccio described the distribution of the interlock equipment around the site and the major requirements for the supervision layer.

Near milestones for these systems are first prototypes of the PIC and BIC respectively in Q3/2002 and Q4/2003. However the BIC should be much earlier if the goal of protecting the new SPS east extraction is to be achieved. Interfaces with the control system, radiation qualification and system validation must then be completed before installation ready for commissioning of the PIC in 2005 and the BIC in 2006.

In response to R. Gavaggio B. Puccio pointed out that the slides are simplified and that some clients of the BIC also receive the Beam Permit signal; the vacuum system needs the information that the beam is dumped.

C-H Sicard asked if more information concerning the work to realise was available. B. Puccio replied that this was being discussed as an activity to be launched by the future AB-CO group. R. Schmidt suggested that, from String experience, the supervision might take 6 months to develop, communications had not required effort but the PIC might need 1 MY to program.

P. Gayet suggested that local logging should be done at the PLC level to improve the reliability of the chain.

E. Ciapala asked about how fault sequences would be registered and what was the associated timescale. R. Schmidt said that time stamping for the BIC must be at the level of a μ s and hardware will be used to latch sequences. Information from different crates would be compared by locally latching the 10 MHz beam permit loops.

6. AOB

R. Schmidt remarked that each of the 3 systems covered in this meeting needed a database description of the power circuits. He proposed that these users should meet to discuss and compare their requirements.

ACTION: R. SCHMIDT

Long-Term Actions	People
Underground Control Rooms requested	R. Lauckner
Establish Post-mortem sub-project	R. Lauckner
Clarify Middleware Services to be used by LHC-CP	Core Team

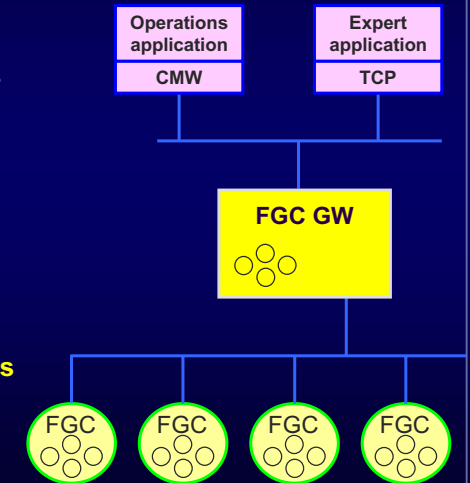
Reported by R. Lauckner

The LHC Function Generator/Controller (FGC) Gateway

- u What the FGC gateway must do
 - u **How it will do it**
- u Gateway between IP LAN and WorldFIP
- u Receive Date/Time and Events
- u Support Real-time Control and Publication
- u Manage FGC software & configurations

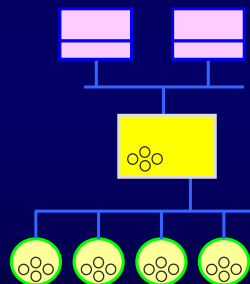
Gateway between LHC IP LAN and WorldFIP Fieldbus

- u Provide the link between Applications and the FGCs for Command/Response
 - u For middleware clients (LHC operations)
 - u For TCP clients (Expert interfaces)
- u Support Device/Property Model
 - u Set Device:Property Values
 - u Get Device:Property



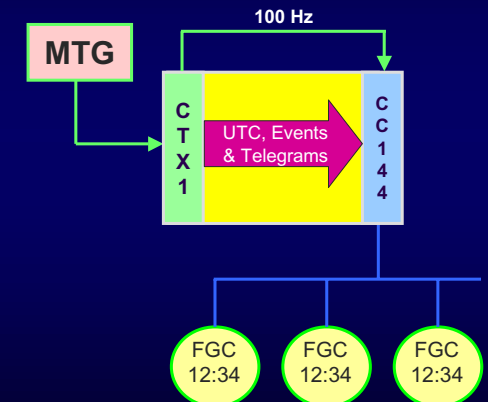
Gateway between LHC IP LAN and WorldFIP Fieldbus

- u **Asynchronous operation:** Commands can be sent to up to eight FGCs simultaneously
- u TCP server
- u CMW server
- u Device name resolution for FGCs
- u Contains device with GW properties, e.g. event table



Receive and distribute Date/Time and Events

- u Receive GMT signal from MTG via CTX1
 - u UTC
 - u Machine Events (Start Ramp...)
 - u Telegrams (Energy, Intensity)
- u Generate 100 Hz trigger pulses for CC144 WorldFIP interface



Support Real-time Control

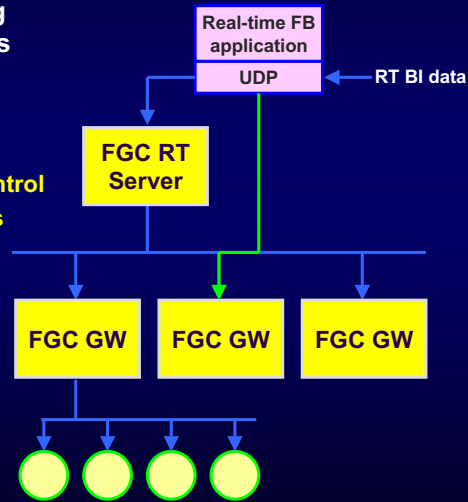
- u RT control allows one floating point value per FGC per 10 ms

- u **FGC RT Server**

- u Provide routing
- u Provide exclusive access control
- u Use UDP for link to Gateways

- u **FGC can use the RT value**

- u As a gain factor
- u As an offset
- u Directly as the reference



Support Real-time Status Publication

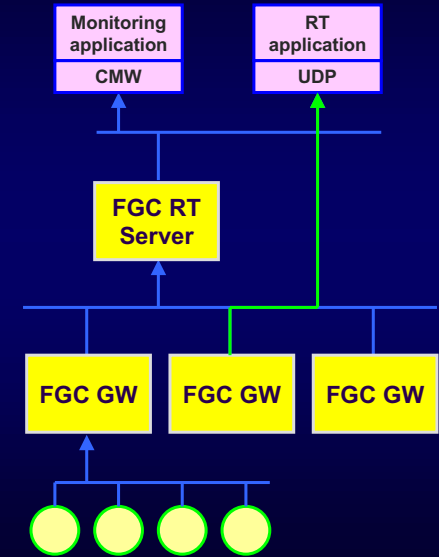
- u 32 bytes of status from every device at up to 100 Hz

- u Contents of status block depends upon the device class

- u Direct UDP subscriptions for high speed applications (> 2 Hz)

- u CMW subscription for low speed applications (< 2 Hz)

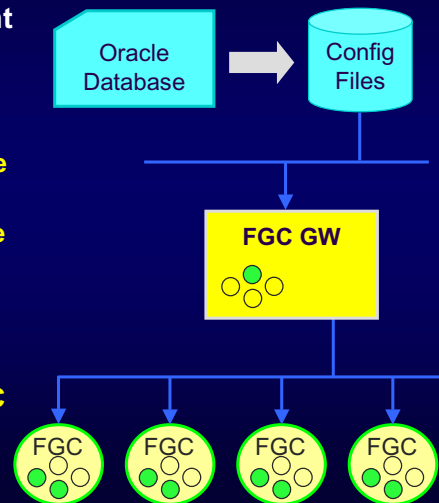
- u GW will include circular post-mortem buffers



Configuration Management

- u Some properties are persistent and part of the *configuration*, e.g. circuit characteristics, ADC calibration...

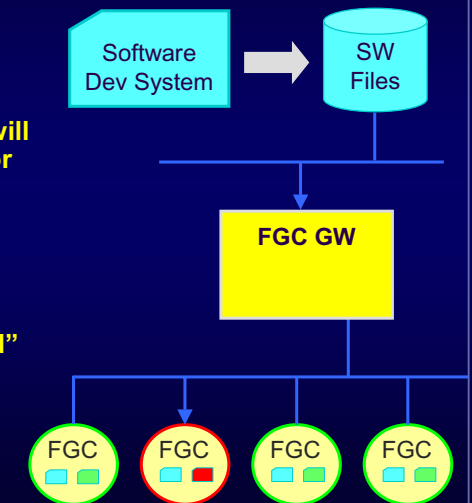
- u Values will be stored in Oracle
- u Working values will be stored in files, generated from Oracle
- u When an FGC needs reconfiguring (e.g. after being replaced), the Gateway will automatically send the values from the config file to the FGC



Software Management

- u The Gateway will check the FGC software version after each FGC **reset**

- u If the SW needs updating it will transmit the latest version for that class of FGC (~30s)
- u Each FGC has two Flash memories for code – while running from one, the other can be reprogrammed
- u The new code can be “tested” and if it fails, the FGC watchdog will restart the old code



Identity Management

u All FGC boards, DCCTs, ADCs and Voltage Source Modules will be identifiable via a special Dallas-ID bus

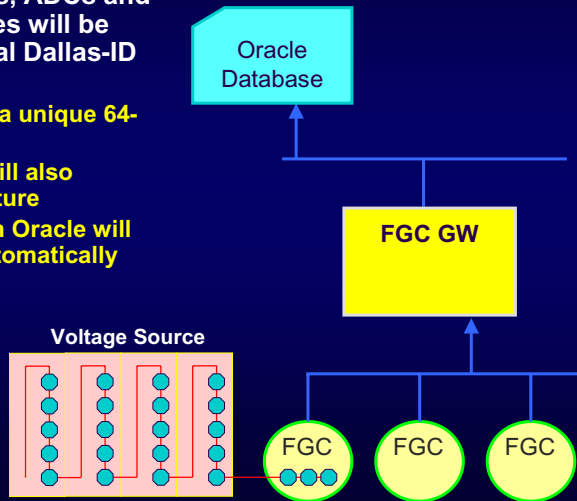
u All Dallas chips have a unique 64-bit number

u In some cases they will also measure the temperature

u Complete inventory in Oracle will be kept up to date automatically by the Gateways

u About 40'000 items will be tagged within the complete LHC powering system

u Module Identity will be central to inventory management



FGC Device:Property Model

u What is an FGC Device?

u Named entity containing properties and a command parser supporting set or get

u Belongs to a class

u Publishes a data set in real time

u Every FGC and Gateway is/contains a Device

u What is an FGC Class?

u A type of device designed to fulfill a specific function (Gateway, Power converter FGC, RF FGC)

u Defines a list of properties

u Defines a published data set

u No Class inheritance

FGC Device:Property Model

u What is an FGC Property?

u Named entity containing typed data array and set and/or get methods

u Has a maximum number of elements (array size) and current number of elements

u May be a simple type (e.g. INT32U, FLOAT) or composite (e.g. CAL which has an INT32S and a FLOAT)

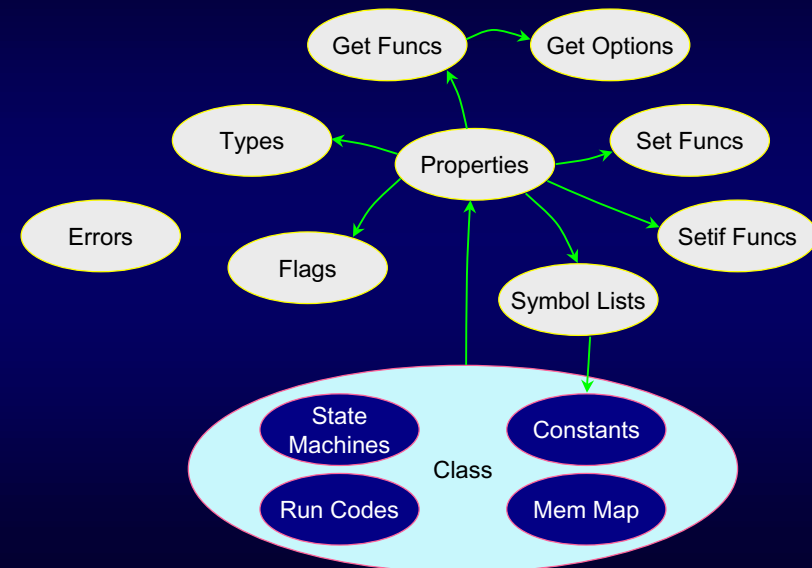
u May be persistent (configuration properties)

u May be published

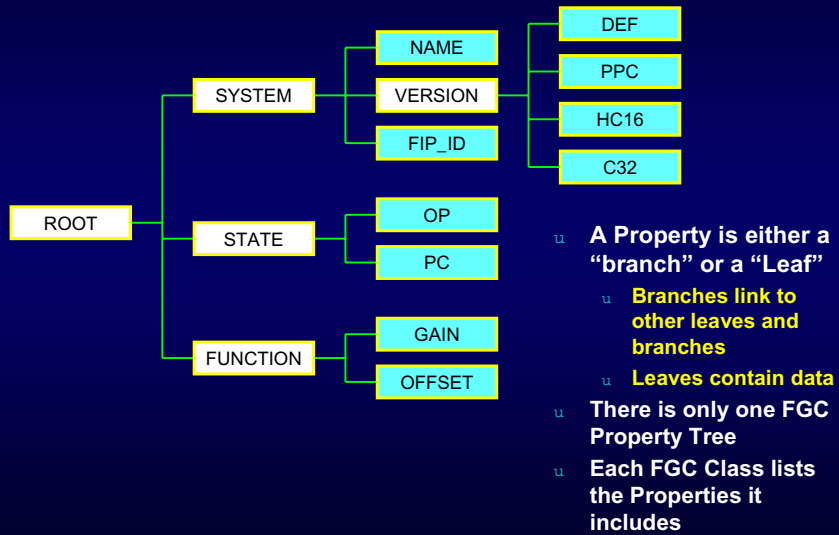
u May be visible via CMW

u Included in one or more classes

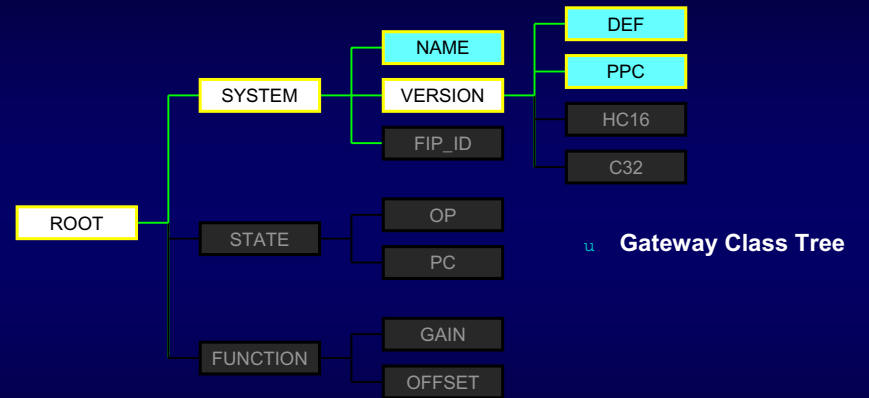
FGC Device:Property Model



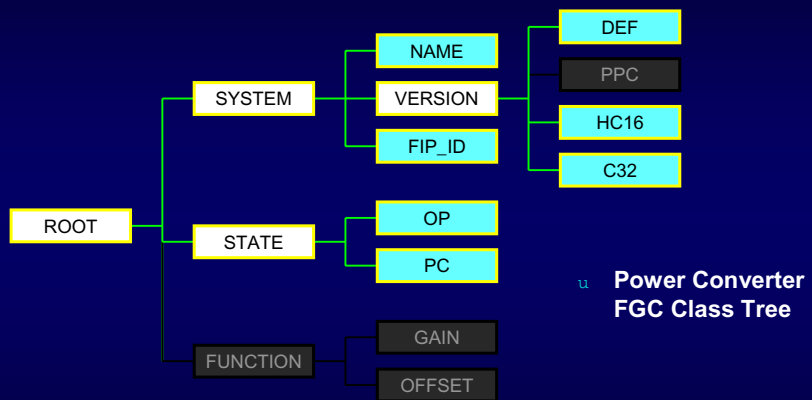
FGC Property Naming



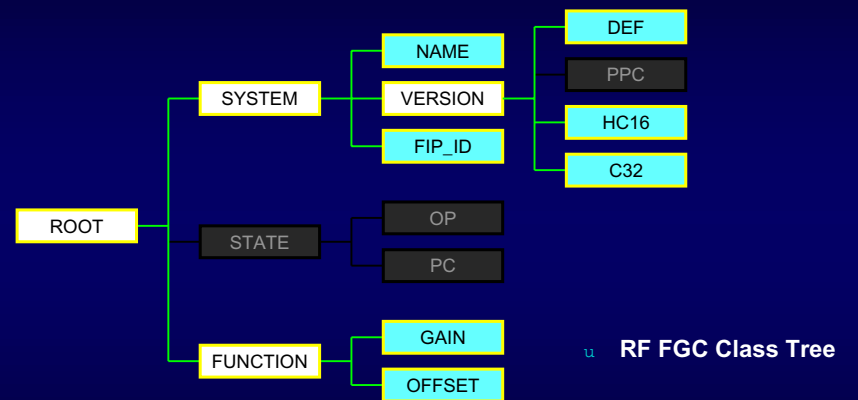
FGC Property Naming



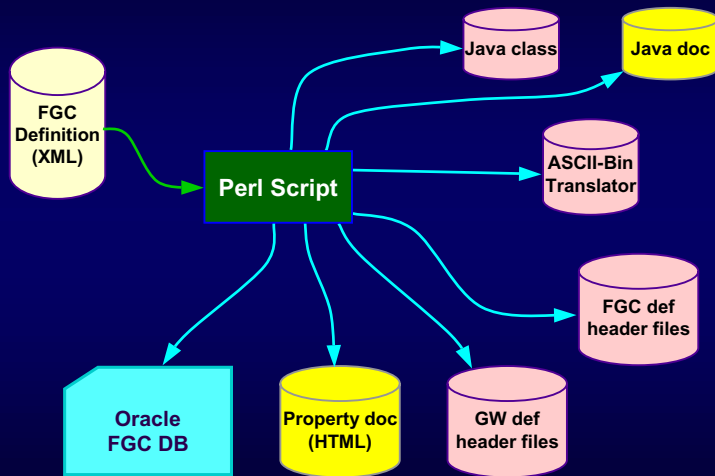
FGC Property Naming



FGC Property Naming



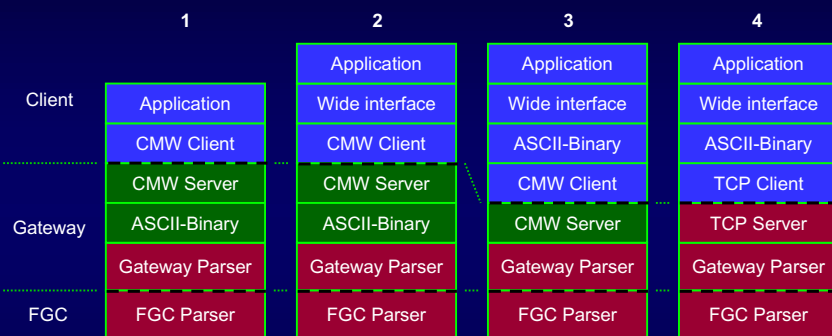
The use of Perl offline



Open Questions

- u The FGC Device parsers work with ASCII commands
 - u **At which level should the translation to binary be done?**
 - u 1. In the Gateway? – Bottleneck
 - u 2. In the Client? – CMW device explorer won't work
- u Does SL/PO provide a Java Class with explicit set and get methods for every property visible via the CMW?
 - u **Wide interface allows compile time type checking**
 - u **Class could include ASCII-Binary translation**

Alternative Architectures



- u Many alternatives can be considered – each with benefits and problems
- u Prototyping is essential – multiple solutions are possible with code generation from XML



Conclusions

- u The FGC Gateway will have many different roles
 - u **Gateway for Commands, Real-time control, Publication and Machine Timing**
 - u **FGC Software, Configuration and ID Management**
 - u **Terminal server for FGCs**
 - u **Post mortem**
 - u **Alarms (via top level RT data server)**
- u Extensive use of XML allows Gateways and FGCs to present a uniform Device:Property interface
- u Special expert and RT applications need direct TCP/UDP communications
- u Operational applications will use CMW and perhaps an automatically generated wide Java API

DQAMC/DQAMS requirements

- n Spread all over the tunnel and underground area
- n Acquiring data at max 100Hz, time stamping of the data at 1ms precision
- n Internally buffering the data (FIFO buffers), frozen if detection of an event
- n WorldFIP: 100ms micro cycle, max 50 nodes/bus
- n Synchronization of the time via WorldFIP
- n On redundant UPS (10min autonomy)
- n High availability
- n Local evaluation of the power permit
- n Test functionality by simulating a quench and observe responses from:
 - n The quench detectors and the quench heater power supplies
 - n The energy extraction units
- n Different configuration, downloaded from DQGTW

2nd July 2002

LHC-CP: QPS controls requirements

5

DQGTW requirements

- n Located in alcoves, UAs and RRs, remotely/locally accessible
- n Master of maximum 2 WorldFIP.
 - n Maximum 10Kb of data from each DQAMC/DQAMS
- n LHC time synchronization: 1ms.
 - n Forward it to the DQAMC/DQAMS
- n On UPS (10min autonomy)
 - n Handle 100*10Kb data in less than 10min in case of power loss.
- n Connected to Ethernet
 - n Shall run without the network
 - n Shall store locally data in case of network problem: LHC Logging, etc.
- n Handle QPS expert command:
 - n Test mode propagated to DQAMC/DQAMS (one/all/selected)
 - n Access to all the handled data
- n Interfaced to LHC Alarm, Post-Mortem, Logging, MPS (power permit), supervision, LHC operators

2nd July 2002

LHC-CP: QPS controls requirements

6

QPS requirements (1)

- n QPS Supervision:
 - n Used by QPS expert for commissioning and during operation
 - n Console/computer in the control room
 - n Not on UPS so far (is Ethernet on UPS?)
 - n Graphical interface for the QPS expert
- n Part of QPS control ready for hardware test on surface
 - n Basic supervision
 - n DQGTW
 - n Configuration database
 - n Hardware database (traveler)
- n QPS control must work since the beginning of the commissioning

2nd July 2002

LHC-CP: QPS controls requirements

7

QPS requirements (2)

- n QPS equipment will be deployed in stages (sector by sector)
 - n All installed equipments stored in the hardware database
 - n Calibration data and configuration data stored in the configuration database
- n QPS expert shall have access to LHC Alarm, Post-Mortem and Logging for the event diagnostic
 - n Access to all the QPS archived data
- n Software developed once and configurable
- n Long term maintenance
 - n Hardware, software, etc.
 - n Upgrades
- n QPS will provide:
 - n Data for LHC operators
 - n Procedures in case of quench or other event

2nd July 2002

LHC-CP: QPS controls requirements

8

QPS: some numbers...

- n 2077 DQAMC/DQAMS
- n 59 WorldFIP field buses
- n 35 DQGTWs (+2 for test and development)
- n ~70000 data channels (analog and logic)
 - n 21% commands from DQGTW to DQAMC/DQAMS
 - n 79% data from DQAMC/DQAMS to DQGTW
 - n 27% analog
 - n 75% to logging
 - n 45% generate an alarm, not all of them to LHC Alarm System
 - n Data for post-mortem: To be defined
- n Logging and Supervision: magnitude of change for recording to be defined
- n Data quantity in case of quench: maximum of 10kBytes per DQAMC/DQAMS

QPS installation planning

- n Hardware test of equipment for sector 7-8 on surface [01/2004 to 05/2004]
 - n Mount the DQAMC/DQAMS and hardware
 - n Test the DQAMC/DQAMS: test mode, etc.
- n Installation in tunnel for sector 7-8 [05/2004 to 12/2004]
 - n Installation and test of the QPS racks
- n Commissioning sector 7-8 [from 03/2005]
 - n Full test of QPS
- n And then the other sectors...

QPS needs [and when] (1)

- n Configurations within LHC Operation database [01/2004]:
 - n Store the configuration of DQAMC/DQAMS, DQGTW, etc.
 - n List of signals
 - n Calibration data of the signals
- n Hardware database [01/2004]
- n WorldFIP [05/2004]:
 - n QPS needs already given to WorldFIP group
- n Ethernet [05/2004]: in alcoves and UAs-RRs
- n Computers [05/2004]:
 - n DQGTW in alcoves and UAs-RRs
 - n Console for QPS experts, supervision, etc. in a place to be defined
- n LHC Timing [05/2004]: 1ms in alcoves and UAs-RRs
- n Voice communication and UPS [05/2004]

QPS needs [and when] (2)

- n LHC Alarm
 - n Interface [01/2004]: for the software development
 - n Operational [05/2004]: commissioning
- n LHC Logging:
 - n Interface [01/2004]: for the software development
 - n Operational [05/2004]: commissioning
- n LHC Post-Mortem:
 - n Interface [01/2004]: for the software development
 - n Operational [05/2004]: commissioning



QPS manpower needs [and when]

- n Development
 - n DQGTW: 1 year of work [09/2002 to 05/2004]
 - n Full development, test and validation
 - n Generic configuration
 - n QPS Supervision: 1 year of work [07/2003 to 03/2005]
 - n Pre-commissioning and commissioning
 - n Interface to required databases (collaborations with other groups)
- n Support and maintenance provided by the specific teams are fundamental
 - n Deployment of the DQGTW and Supervision for the other sectors
 - n Long term maintenance



Milestone-deliverables

- n DQGTW:
 - n Ready for surface tests [01/2004]
 - n Installation, cabling, hardware tests
 - n Corresponding to 80% of full functionalities
 - n Full functionalities ready for tunnel installation [05/2004]
- n Supervision:
 - n Basic applications for hardware tests on surface and tunnel pre-commissioning [01/2004]
- n QPS controls ready for commissioning 7-8 [03/2005]
 - n Commissioning of the whole QPS control chain
 - n All functionalities available
- n Deployment for the other sector tests:
 - n Creation of the configurations by QPS experts
 - n Download of the configurations
 - n Development/configuration of the graphical interface of the QPS for the other sectors.

Machine(s) Interlocks:

Architecture
Milestones
Expectation to Controls

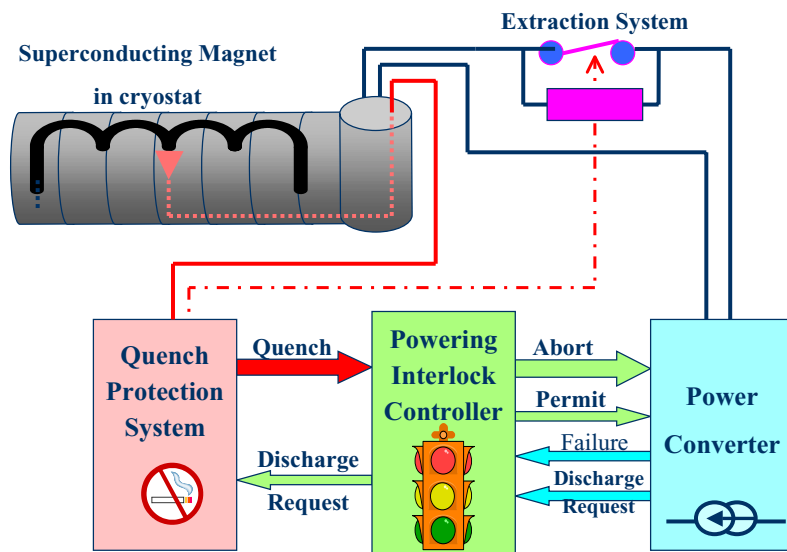
Relationships



Controls Expectation for the Machine Interlocks by R.S & B.P

LHC-CP of July 2, 2002

Interlock basis

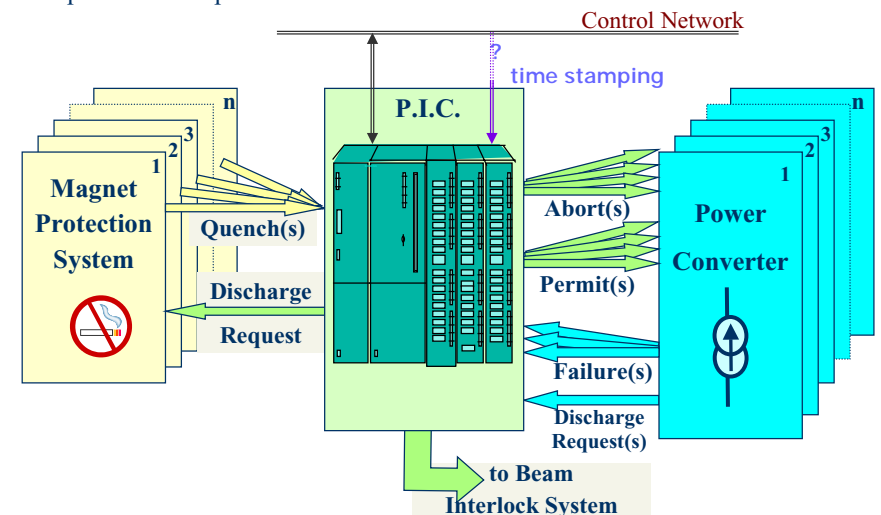


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Powering Interlock Controller

- w Each PIC manages a various number of electrical circuits with different interlocks
- w Response time expected ~ several mS

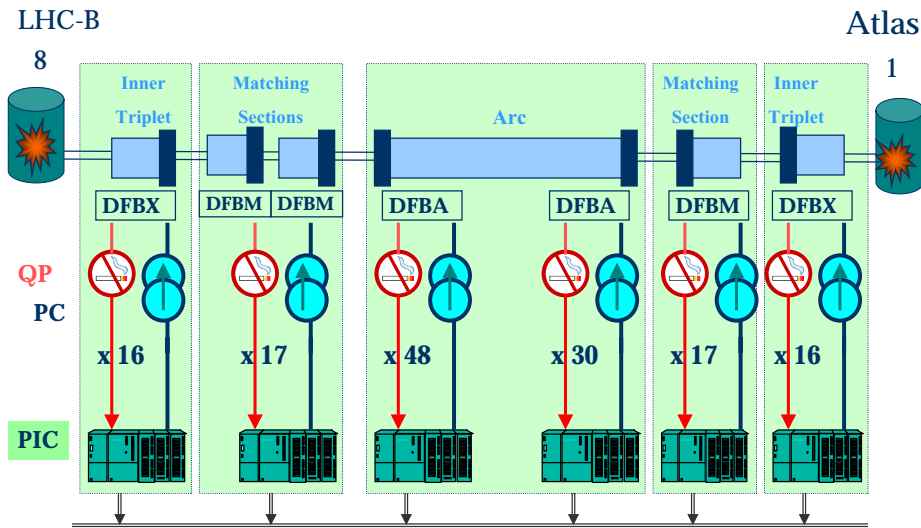


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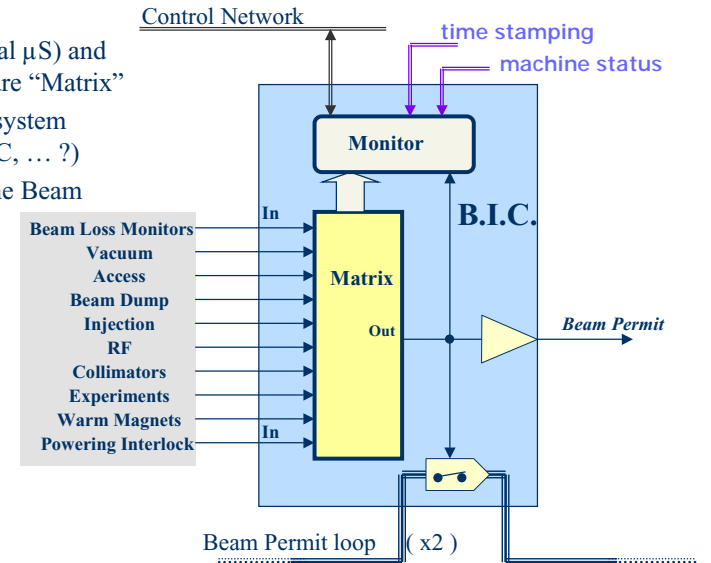
Powering sub-sectors

(example with the sector 8-1)



Beam Interlock Controller

- w Must be fast (several μ S) and reliable => Hardware "Matrix"
- w Embedded in host system (VME, C-PCI, PLC, ... ?)
- w Fast link to carry the Beam Permit information

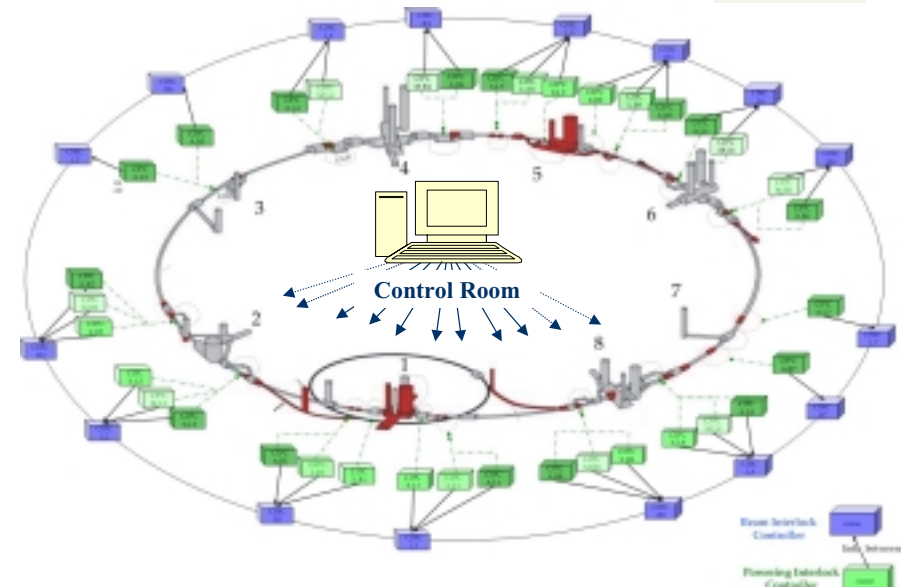


Layout of the Beam Interlock System

- w 16 B.I.C. units
- w 2 fast links
- w if one loop broken => Beam Dump

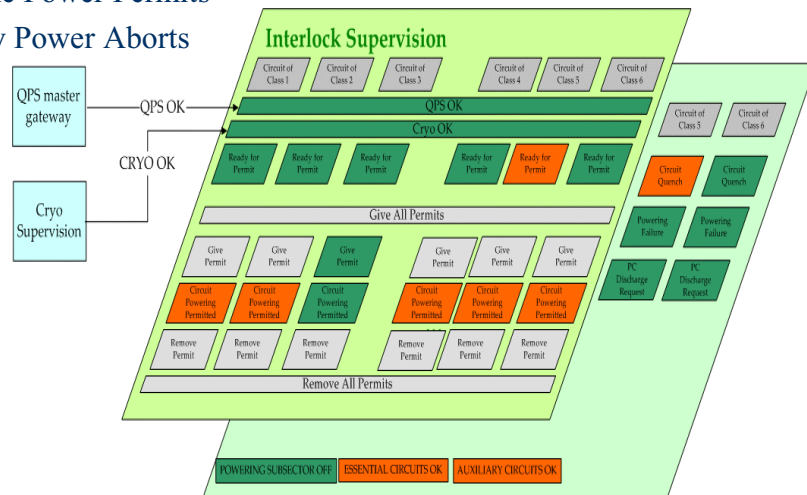


General Layout of the 2 Interlocks Systems



Powering Interlock Supervision

- w Visualize Powering Sub-sectors status
- w Give the Power Permits
- w Display Power Aborts



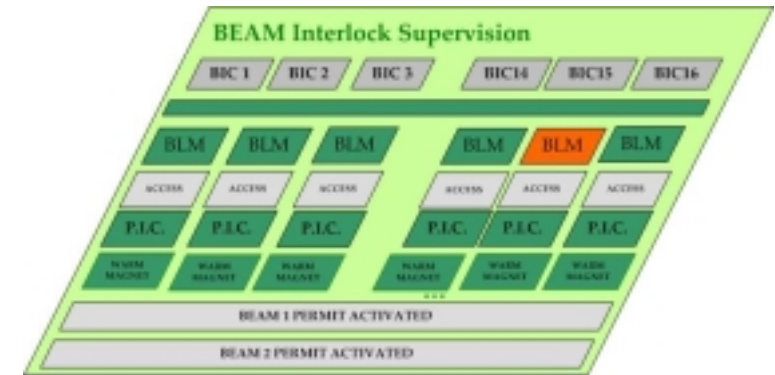
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9

Beam Interlock Supervision

- w Put on view of the Interlock inputs
- w Visualize the source in case of the Beam Dump
- w Display the Beam Status
- w Give the Beam Permit

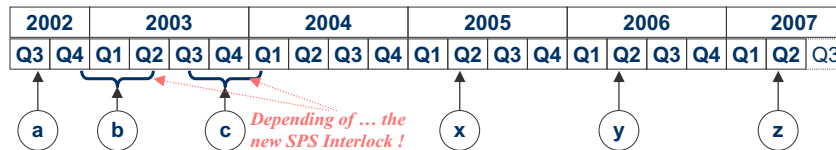


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10

Milestones



- a) Q3/2002 : First PIC prototype ready (with internal software)
- b) ~ Q1/2003 : Choice of the host platform for the BIC Matrix
- c) ~ Q4/2003 : First BIC prototype ready (earlier if SPS Interlock project has started...)

for the Powering Interlock (installed in the RR): Analyse radiations influence for both systems; Validate technical choices then Study the safety integrity level, Define data base for configuration, Choose Supervision, decide a Middleware(?), Write application programs, Finalize Post-Mortem interface then... start installation in the machine, debugging and commissioning.

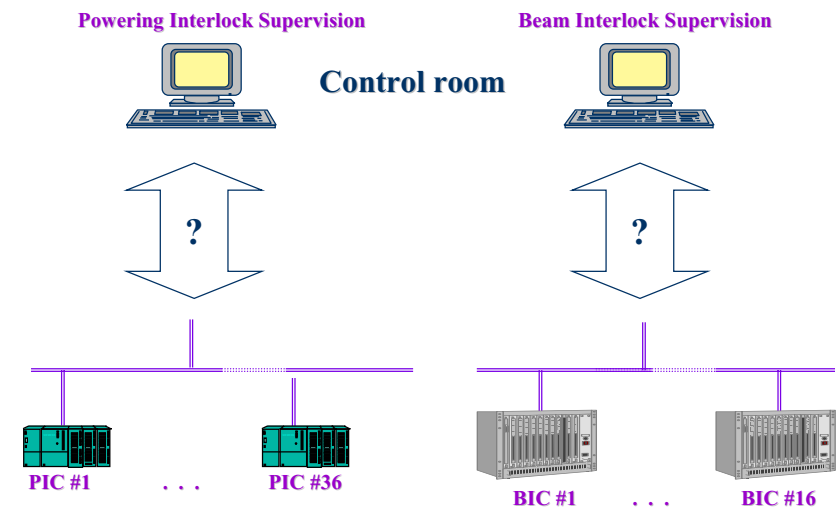
- x) March 2005 : Powering Interlock mandatory for Sector 7-8 Hw commissioning
- y) April 2006 : Beam Interlock system ready for Injection test
- z) April 2007 : First beams

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11

Needs expected

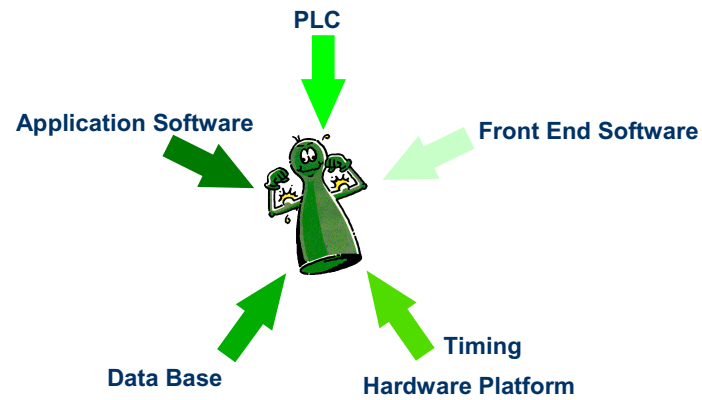


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12

Supports expected from CO



Conclusion

All elements of the Controls group will be involved.

Deadlines are not April 2007 but before:

- _ the Sector test starts in April 2005 !
- _ must foresee several months for the commissioning...

Challenge for A&B/CO to achieve it in time

Opportunity to show to others its competence and its efficiency.