SPS Hardware Interlocks

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for the 'SPS interlock ***study*** team' :

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- **Motivations**
- **Requirements**
- **Status and Outlook**

Hard versus Soft

- Hardware interlocks :
  - § are triggered via hardware connections.
  - § are the last line of defense for 'dangerous' situations.
  - § must be fail-safe.
  - § are required for fast decisions.
  - § do not involve (complex) central processing.
- Software interlocks :
  - § managed by a central "program".
  - § not fail-safe, but more flexible.
  - § provide redundancy & diagnostics.

Software interlocks are part of the SPS2001 project !

Motivation & requirements

In the LHC & CNGS area, the hardware interlock system
- § must support fast cycle changes.
- § requires additional inputs : beam quality, LHC inputs…
- § must handle fast extractions !

Not full-filled by the existing system !

Main (Sub-)Components :
- § The SPS emergency beam dump.
- § The extraction interlocks for **CNGS, LHC and FT beams.**

LHC developments

The LHC power & beam interlock systems are also in the design phase.

A **collaboration** was started between SPS & LHC :
- § To exchange experience.
- § Avoid duplicated efforts.
- § Adopt common solutions (if possible & practical).

attempt to move towards homogenous systems for both machines, at least as far as this makes sense !

Fast cycle changes

Fast Cycle changes imply that :

- Settings for different cycles must be stored in the front-ends,..
- All systems must be ready to execute any stored cycle.
- The information about which cycle to run is distributed by the machine timing system.

applies also to the hardware interlock logic !

we must consider fail-safe handling of machine timing inside many systems generating hardware interlocks & inside the interlock system itself !

SPS Emergency Beam Dump

The present SPS beam dump system does not know about SPS cycles, but :

- Some form of cycle handling is already performed by the systems providing some input channels (Beam losses).
- Clean cycle handling is limited so far due to missing information (precise beam type…)

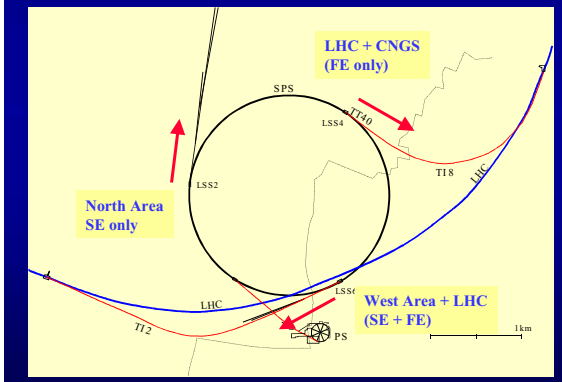
  Timing system must provide more info in the future !

For the future

- The present emergency beam dump system could **"survive"** into the multi-cycling area, but :
  - spare parts are rare.
  - not much room for new inputs.
- A new system must be put in place in the coming years.

Extraction Interlocks

The extraction interlock system must know which cycle is played because the extraction channels are shared :



- LSS4 : CNGS/LHC (TI8).
- LSS6 : FT/LHC (TI2).

Interlock conditions must change with cycles !

Status

The interlock situation has been reviewed with the "actors" that are involved today (BI, BT, PO, CO) to identify

- Present limitations.
- Future developments.
- Critical issues :
  - Timing.
  - Power converter surveillance (inside ROCS ?).
  - Vacuum (sectorization).
  - Beam quality handling.
  - LHC interlock & beam request handling.

Some ideas have emerged, but more work is required before a solution emerges.

Timescales & outlook

- 2002 : proposal for a conceptual design.
- Summer/fall 2003 : extraction tests TT40 / TI8.
  - Ideally : test of a 'meaningful' prototype.
  - It is not clear if a prototype can be build within that timescale !
- Most urgent problems / decisions :
  - NO manpower is presently available to build the SPS system.
  - A proposal to form a single interlock section for all machines has been made, but the 'home-group' and manpower resources of this section are not finalized…