The Fourth LHC Controls Project Workshop
12th – 13th June 2003

Friday 13th June:

Session – 3 Common Controls Facilities

LHC Timing

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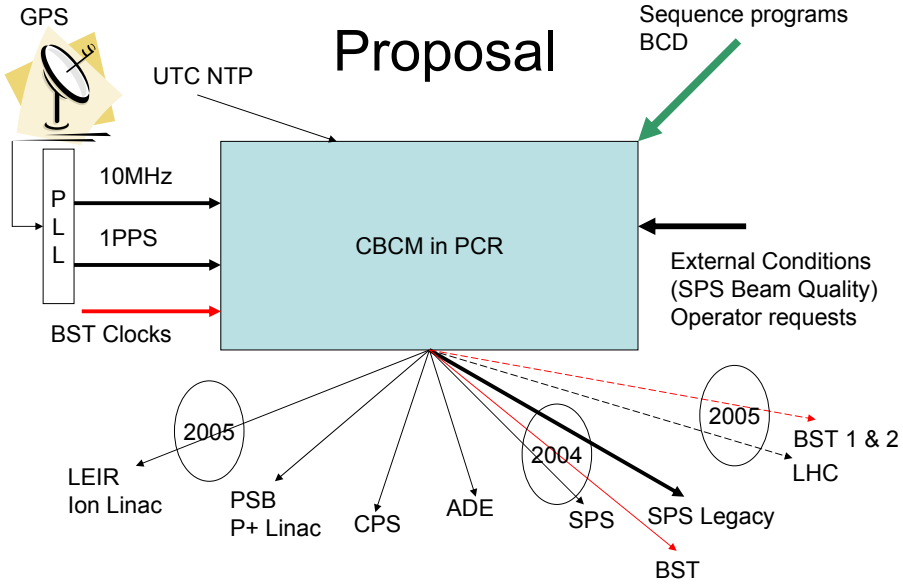
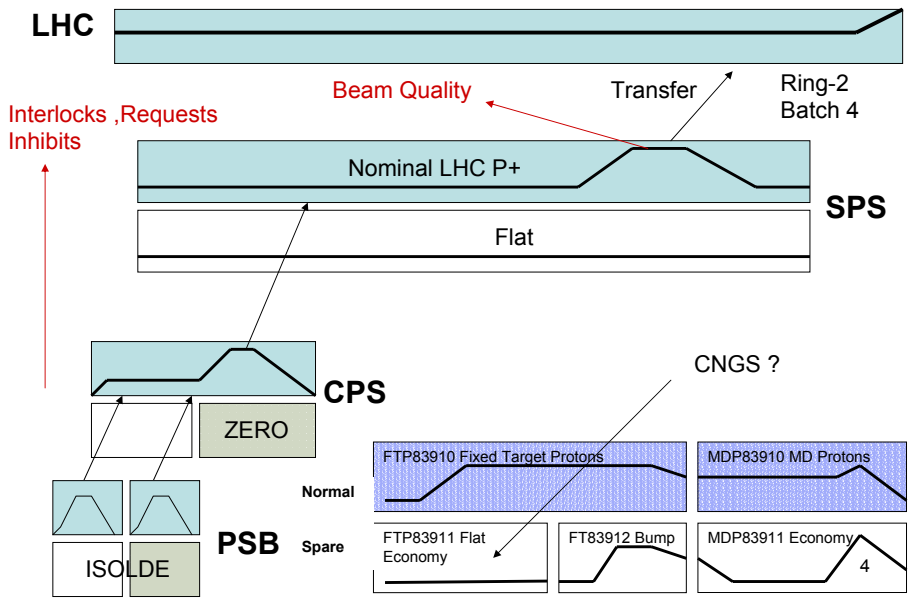
What is LHC timing

- All the CERN accelerators will share the same Lego for timing. Generation, Transmission, Reception hardware. The software drivers and high level equipment access is also shared.
- Today the big effort is for the SPS, and this work can be directly applied later to LEIR and LHC
- This will permit SPS/LHC people to gain some experience with the CBCM in 2004/2005. This will be a very valuable exercise for us all.

Proposal



Sequence programs BCD

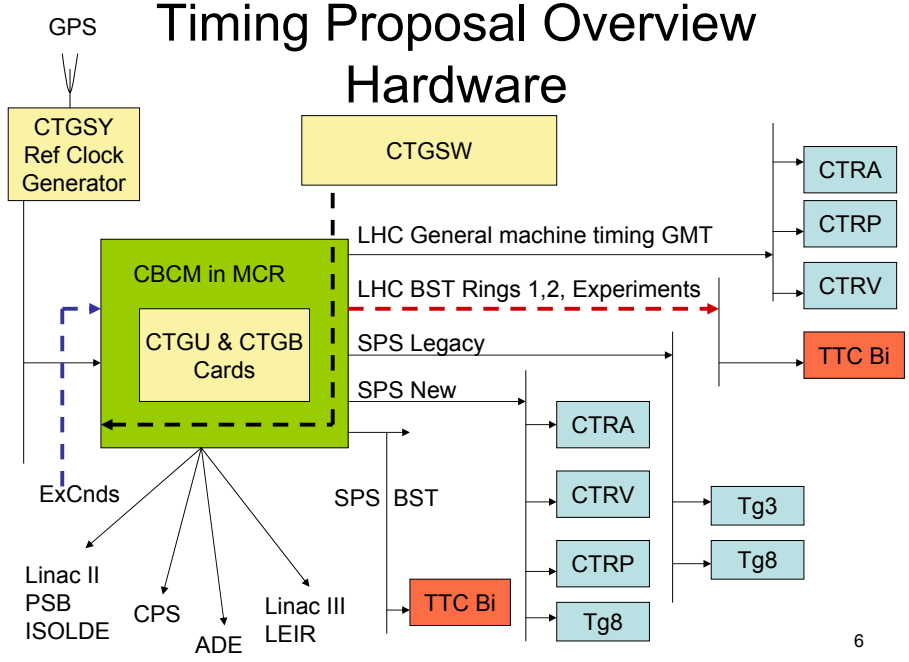


The principle

- LHC GMT driven from CBCM
- LHC BST driven from CBCM
- Same hardware used in PS and SPS
- Same software used in PS and SPS
- Strongly UTC time based
- Telegrams
- Strongly coupled with the SPS during beam transfers

I.E. LHC is just like the other machines as far as the timing is concerned

Timing Proposal Overview Hardware



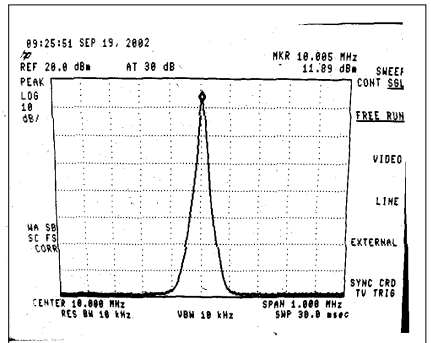
Hardware Developments

- CTRA VME Timing receiver designed specifically for gateways. May not be used in a gateway, but we have added generalities.
- Hardware and software ready and tested.
- Waiting production run of 30 modules.
- Can be used in simple applications on any accelerator, interrupt RT task, read telegram, output an event, read UTC time.
- Has a simple DPLL on board
- Delivery September 2003 (30 modules)

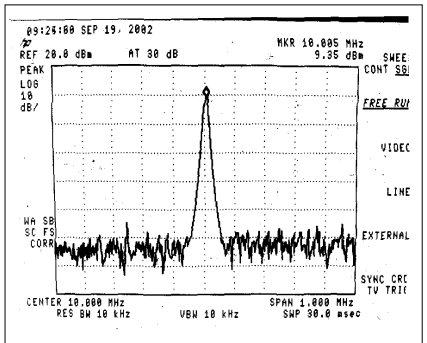
Hardware developments

- CTRP Timing receiver module in PMC format.
- Advanced timing card with 5 x 32 bit, 50 MHz fully programmable counters.
- Full support for multi-cycling.
- High precision TDC with better than 1ns resolution based on the HPTDC CERN chip, alternatively on the 40MHz clock, 25ns.
- On board T/VXCO regenerates the 40MHz, we hope this will solve the RF 10MHz requirement
- Delivery: Hardware and Software Oct 2003

10 MHz Reference (cont'd) Spectral purity needed by SPS and LHC RF systems.



Local FC BA3 reference



CERN wide 10 MHz as received in FC BA3

Hardware developments

- CTRV, VME version of the CTRP
- 8 Counters
- Front panel on module provides 50 Ohm TTL connectors
- Fully replaces a Tg8 and then some.
- Delivery during 2004

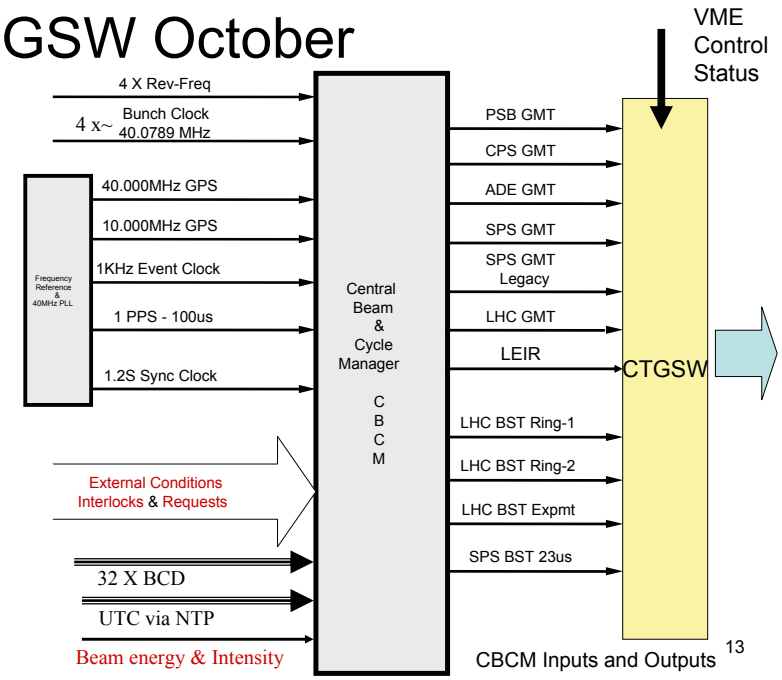
CTGB Prototype

- Prototype BST master card based on the same PCB used in the CTGU.
- Hardware PCB, VHDL, Driver, Library, and Assembler / Disassembler application written. Testing now.
- Delivery 2/3 weeks
- This is a prototype based on the small FPGA and 16 VME P2 connections.
- Big version is in the drawing office. August 2003

CTGU

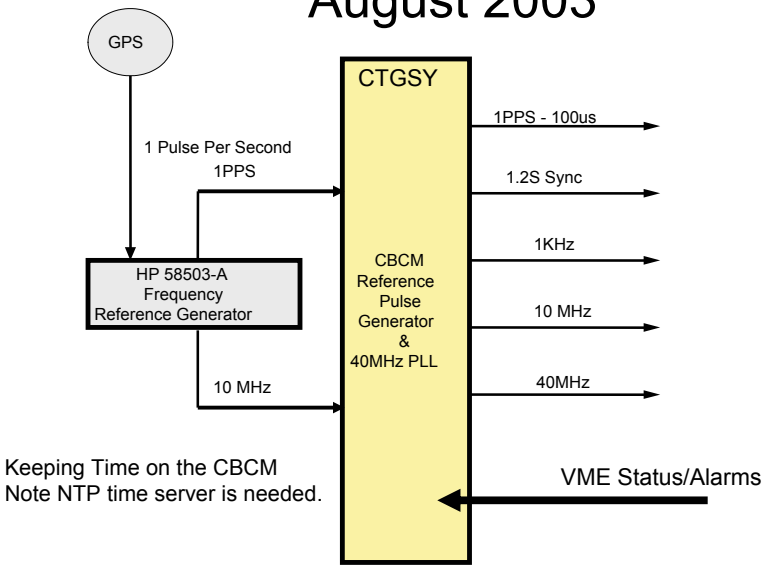
- Like the CTGB but drives a GMT timing distribution cable.
- Hardware and software ready August

CTGSW October



CBCM Inputs and Outputs

Keeping Time with UTC CTGSY Card August 2003



Keeping Time on the CBCM
Note NTP time server is needed.

Hardware developments

- ECL, TTL, RS485 -> Optical
- Optical -> ECL, TTL, RS485 (September)
- Digital transmission of data, such as external conditions, beam energy/intensity. Delivery in 2004
- Optical, ECL, TTL fan outs

Signals to be delivered Bunch and Frev clocks

- 40.08MHz Bunch clocks (2/3 off)
- 11KHz 89us Revolution frequencies (2/3 off)
- These will be delivered across the TTC under the BST system. Or by TTC alone.
- On separate fibers
- AB/CO will pick them up in SR4
- Local survey in SR4 before transmission
- BST delivery is under AB/BI responsibility

Signals to be delivered
LHC Injection & SPS Extraction Pulses (4 in total)

- Generated in FC SR4 and BA3 on two separate cables, one for each ring. (In principle they are the same)
- Needed by Etienne (SR2/SR8) and Jean-Jacques (where? which ?)
- AB/CO takes them from SR4 to the users
- Precision/Stability limited by normal optical fibers mono mode.

Signals to be delivered
General Machine Timing

- Responsibility of AB/CO, available in all surface buildings, and as required.
- Optical long distance, RS485 short hauls.
- Contains Telegrams, UTC time (1/25ns resolution), Timing events, 40MHz master clock (4 x 10.0000 MHz). 1KHz events containing machine time (2^24 ms = 4.66 Hours) We can extend the range by incrementing every 2nd tick.
- Contains the 1PPS

Signals to be delivered
10MHz

- Using either a CTRP or a CTRV
- Spectral purity to be measured, if not good enough, install 10MHz system in SR4
- 10MHz is used throughout the PS complex by the RF and TSMs, by the SPS RF, and LHC. The (10MHz x 4) is used to encode the GMT events.

For LTI TT40 Current status

- In charge JB Ribes
- BA4 (RA1348) Timing available
- BB4 (RA0417) Cables in place
- BI HCA442 Timing available
- BI (RA1227) Bunch clock & Frev available
- BT HCA421 (Faraday Cage) GMT, Pre-pulses (CNGS,LHC,SPS) available
- BA4 (RA0904) Timing for SPS interlocks available

All seems OK no big problems

The CBCM

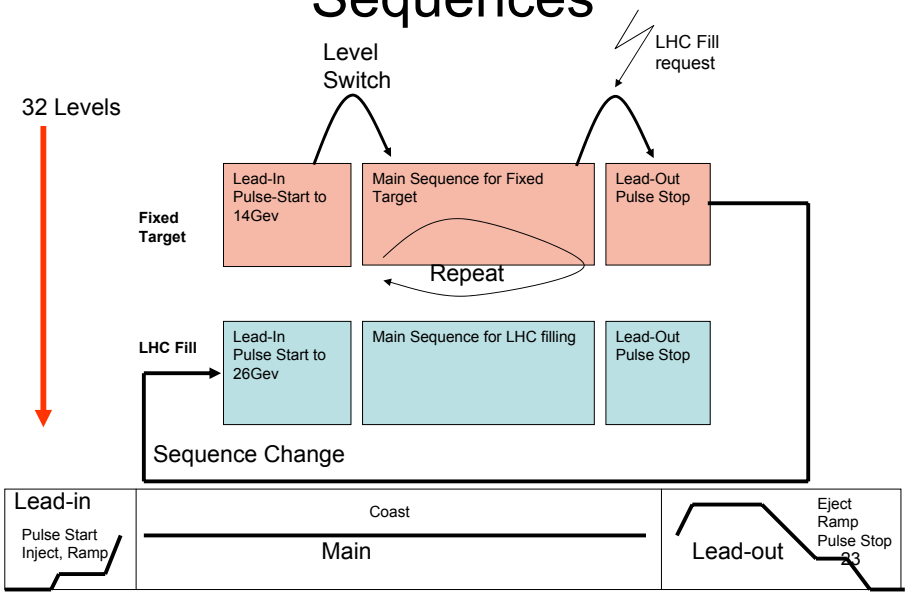
- A large software development is being undertaken, to accommodate the new clients, SPS, LEIR, and LHC. The biggest part of the development is this year.

- SPS startup 2004
- LEIR startup 2005
- LHC startup 2006

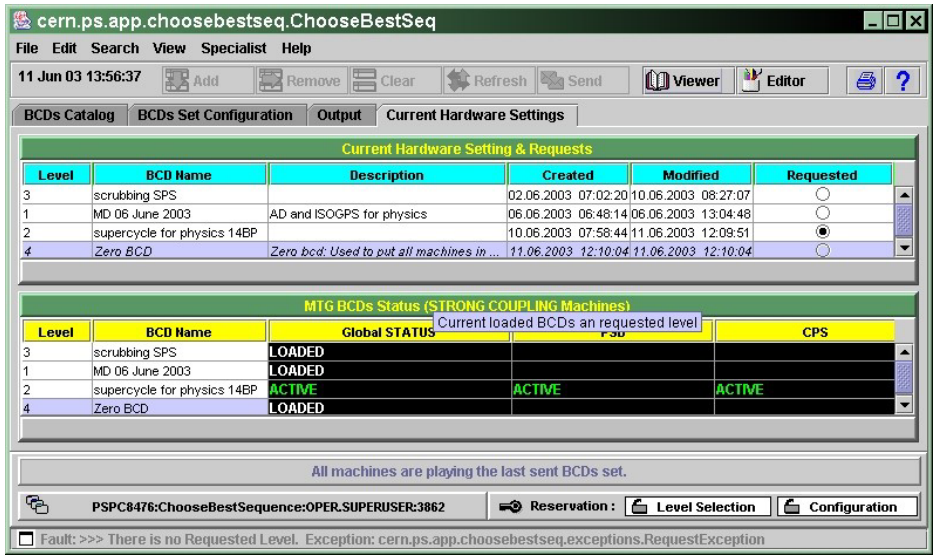
Main features added to CBCM in 2003 for the SPS

- Concept of Lead-In Lead-Out sequence
- 64 SPS cycle instances for multi-cycling
- 8 Full SPS sequences = 24 BCDs
- Choose best sequence program (Java)
- Sequence editor
- Append telegram group to SPS event on request
- SPS timing events
  - **Identify all SPS events, and their behavior, clean up**
  - **Define SPS telegram, and logical events in Oracle**
  - **Build up to 64 SPS cycle instances in up to 8 sequences**
  - **Duplicate some of the MTG legacy behavior**

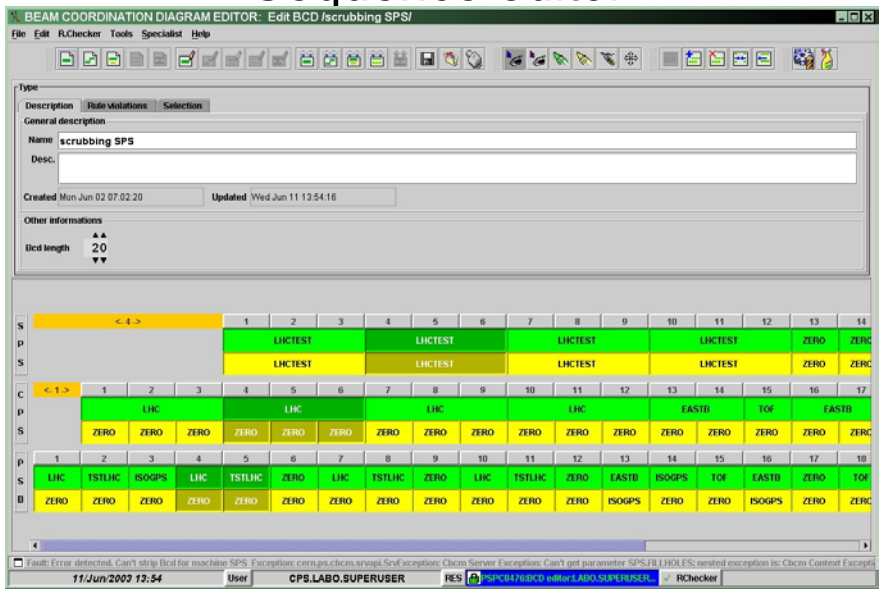
Sequences



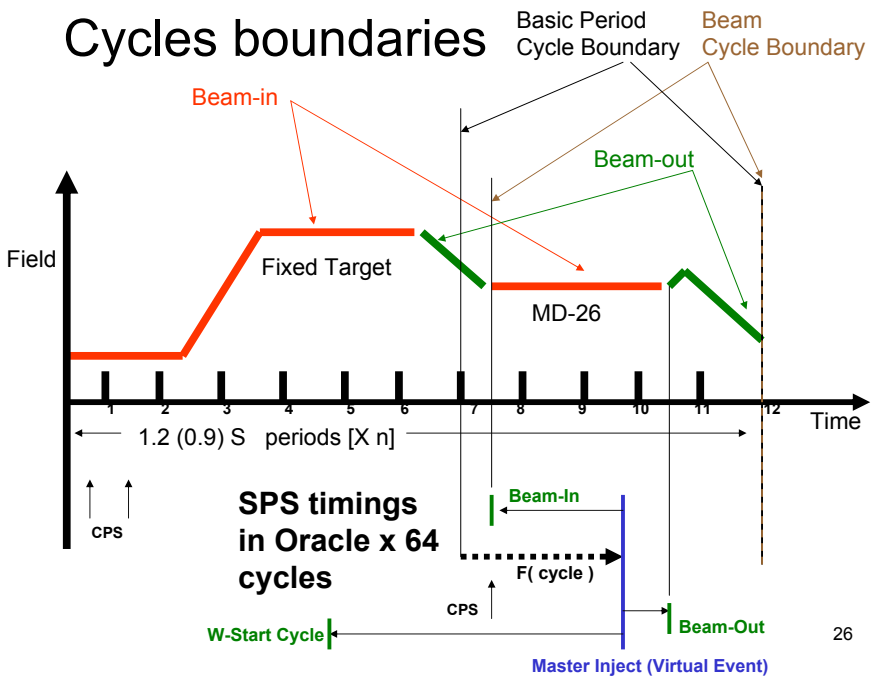
Sequence Manager



Sequence editor



Cycles boundaries



CBCM
Open Questions for LHC

- Pilot beams -> Switch to fill -> Retry/Dump
- SPS interlocks & Beam quality measurements
- LHC Interlocks
- Direct operator inputs, what when how
- Filling sequences, retries, R1B1,R2B2 or what
- CNGS & Fixed Target interleaved
- Beam dump triggering, external event
- Relationship between timing and magnetic cycle.
- We need to know how LHC will be operated to be sure the CBCM implements all requirements